

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **BUILT-IN-SELF-TEST (BIST) FOR MULTI-CHANNEL TRANSCEIVER WITHOUT DATA ALIGNMENT** the specification of which X is attached hereto or was filed on as Application No. and was amended on (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/148,416	August 11, 1999

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status



POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Horace Ng, Reg. No. 39,315
Babak S. Sani, Reg. No. 37,495

Send Correspondence to: Horace Ng TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8th Floor San Francisco, California 94111-3834	Direct Telephone Calls to: (Name, Reg. No., Telephone No.) Name: Horace Ng Reg. No.: 39,315 Telephone: 415-576-0200
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Full Name of Inventor 1:	Last Name: CAO	First Name: JUN	Middle Name or Initial:	
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Post Office Address:	Post Office Address: 1013 Verano Place	City: Irvine	State/Country: California	Postal Code: 92612
Full Name of Inventor 2:	Last Name: MOMTAZ	First Name: AFSHIN	Middle Name or Initial:	
Residence & Citizenship:	City: Irvine	State/Foreign Country: California	Country of Citizenship: United States	
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1 	Signature of Inventor 2 
Jun Cao	Afshin Momtaz
Date 07/03/2000	Date 07/01/2000

50955-DBP.B600

PATENT

ART UNIT 2133

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 30/DBP/B600

SUBSTITUTION OF ATTORNEY WITH
CHANGE OF ADDRESS FOR CORRESPONDENCE
BY ASSIGNEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Broadcom Corporation, assignee of the entire interest in and to each U.S. patent application, identified on Exhibit A attached, under an Assignment recorded in the U.S. Patent and Trademark Office, hereby revokes all previous Powers of Attorney and appoints:

D. Bruce Prout	(20,958)	Harold E. Wurst	(22,183)	Jun-Young E. Jeon	(43,693)
Richard J. Ward, Jr.	(24,187)	Robert A. Green	(28,301)	Peter A. Nichols	(47,822)
LeRoy T. Rahn	(20,356)	Richard A. Wallen	(22,671)	Stephen D. Burbach	(40,285)
Walter G. Maxwell	(25,355)	Michael J. MacDermott	(29,946)	Mark J. Marcelli	(36,593)
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Syed A. Hasan	(41,057)	Cynthia A. Bonner	(44,548)	Richard A. Clegg	(33,485)

all members or associates of or of counsel to the firm CHRISTIE, PARKER & HALE, LLP, telephone (626) 795-9900, as principal attorneys with power to appoint associate attorneys, to prosecute this application and any subsequent application based on the disclosure of this application, and to transact all business in the Patent and Trademark Office connected with this application and any subsequent application.

I hereby certify that this correspondence is being deposited with the
U.S. Postal Service as first class mail in an envelope addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-
1450 on: 10/2/03 D. Prout
(Date of Deposit)

B600:30/DBP

The authority under this Power of Attorney of each person named above shall automatically terminate and be revoked upon such person ceasing to be a member or associate of or of counsel to that law firm.

Please address all correspondence to **CHRISTIE, PARKER & HALE, LLP, P.O. Box 7068, Pasadena, California 91109-7068. Customer Number: 23363**

Broadcom Corporation

Date: September 12, 2003

By


Print Name: Dee Henderson

Title: Intellectual Property Portfolio
Manager

DBP/djp

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CPH/BP No. Application No. Filing Date Title

/BP1646	09/614,308	7/12/2000	Fast Acquisition Phase Locked Loop Using a Current DAC
50944/BP1647	09/540,243/ 6,526,113	3/31/2000/ 2/25/03	GM Cell Based Control Loops
/BP1648	09/632,665	8/7/2000	CMOS Lock Detect With Double Protection
50955/BP1649	09/632,666	8/7/2000	Built-In Shelf Test for Multi-Channel Transceivers without Data Alignment
/BP1651	09/615,033/ 6,389,092	7/12/2000/ 5/14/2002	Stable Phase Locked Loop Having Separated Pole
/BP1651CON	10/095,556/ 6,549,599	3/11/2002/ 4/15/2003	Stable Phase Locked Loop Having Separated Pole
50952/BP1653	09/792,684/ 6,566,971	2/24/01/ 5/20/2003	Method and Circuitry for Implementing a Differentially Tuned Varactor-Inductor Oscillator
50953/BP1653CON	10/407,909	4/2/2003	Method and Circuitry for Implementing a Differentially Tuned Varactor-Inductor Oscillator
/BP1654	09/782,687	2/12/2001	Linear Half-Rate Phase Detector and Clock and Data Recovery Circuit
/BP1655	09/784,419	2/15/2001	Linear Full-Rate Phase Detector and Clock and Data Recovery Circuit
50947/BP1656	09/772,781/ 6,396,894	1/29/2001/ 5/28/2002	Overflow Detector for FIFO
50948/BP1656CON1	10/104,870/ 6,519,311	3/21/2002/ 2/11/2003	Overflow Detector for FIFO
/BP1657	09/788,220/ 6,396,360	2/16/2001/ 5/28/2002	Method and Circuitry for Implementing an Inductor-Capacitor Phase Interpolated Voltage-Controlled Oscillator
/BP1658	09/650,275	8/29/2000	Seal Ring for Integrated Circuits
/BP1660	09/919,636	7/31/2001	Fully Differential CMOS Phase-Locked Loop
/BP1815	09/860,284	5/18/2001	Varactor Based Differential VO Band Switching
50957/BP1818	10/037,897	10/22/2001	Methods and Circuitry for Reducing Intermodulation in Integrated Transceivers

CPH/BP No. Application No. Filing Date Title

/BP1851	09/927,705	8/10/2001	Line Loop Back for Very High Speed Application
50950/BP1883DIV	10/267,054	10/7/2002	Low Voltage Differential to Single-Ended Converter
/BP1885	09/910,436	7/19/2001	Synchronous Data Serialization Circuit
/BP1885CON	10/431,103	5/6/2003	Synchronous Data Serialization Circuit
50958/BP1884	09/955,693	9/18/2001	Linear Phase Detector for High Speed Clock data Recovery
50945/BP2015	09/969,837	10/1/2001	High-Speed Peak Amplitude Comparator
/BP2137	10/159,788	5/30/2002	Method and Apparatus for High Speed Signal Recovery
50956/BP2138	10/092,166	3/4/2002	High Frequency Statistical Loss of Signal Detector
50964/BP2144	10/241,140	9/10/2002	Phase Lock Loop with Cycle Drop and Add Circuitry
50963/BP2233	10/243,086	9/12/2002	Delay Generator
50959/BP2233.1	10/243,281	9/12/2002	Symmetric Differential Logic Circuits
50960/BP2360	10/293,163	11/12/2002	Phase Detector for Extended Linear Response and High-Speed Data Regeneration
50961/BP2361	10/293,624	11/12/2002	Phase Detector with Delay Elements for Optimum Data Regeneration
50962/BP2385	10/335,190	12/30/2002	CDR Lock Detector with Hysteresis
50896/BP2454	09/747,392	12/22/2000	Methods of Recording Voice Signals in a Mobile Set
/BP2445	09/640,963	8/16/2000	Code Puncturing Method and Apparatus
/BP2446	09/636,000	8/9/2000	Maximum Likelihood Sequence Estimator which Computes Branch Metrics in Real Time
/BP2448	10/228,165	8/26/2002	Frequency Offset Correction Circuit for WCDMA
/BP2449	10/242,319	9/11/2002	MPSK Equalizer
/BP2450	10/272,507	10/15/2002	Shifted 8PSK Modulator for EDGE

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